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On the profile of frequency and voltage dependent interface states and series resistance in (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures by using current–voltage (I–V) and admittance spectroscopy methods

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ABSTRACT

In order to explain the experimental effect of interface states (N_{ss}) and series resistance (R_s) of device on the non-ideal electrical characteristics, current–voltage (I–V), capacitance–voltage (C–V) and conductance–voltage (G/ω–V) characteristics of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures were investigated at room temperature. Admittance measurements (C–V and G/ω–V) were carried out in frequency and bias voltage ranges of 2 kHz–2 MHz and (−5 V)–(+5 V), respectively. The voltage dependent R_s profile was determined from the I–V data. The increasing capacitance behavior with the decreasing frequency at low frequencies is a proof of the presence of interface states at metal/semiconductor (M/S) interface. At various bias voltages, the ac electrical conductivity (σ_{ac}) is independent from frequencies up to 100 kHz, and above this frequency value it increases with the increasing frequency for each bias voltage. In addition, the high-frequency capacitance (C_m) and conductance (G_m/ω) values measured under forward and reverse bias were corrected to minimize the effects of series resistance. The results indicate that the interfacial polarization can more easily occur at low frequencies. The distribution of N_{ss} and R_s is confirmed to have significant effect on non-ideal I–V, C–V and G/ω–V characteristics of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures.

1. Introduction

More than three decades; AlGaN/AlN/GaN high electron mobility transistors (HEMT) have attracted much attention due to their promising applications in microwave and optoelectronic devices [1–8]. They have been intensively studied as candidates for high-power devices, as well as for high-speed and high-temperature operations [1–8]. Controlling interface states (N_{ss}) and series resistance (R_s) is an important issue in these structures for high power, high speed and high temperature applications [4]. In order to improve the performance of these devices the effect of surface passivation, dielectric layer (Al_2O_3, Si_3N_4) insertion, surface treatments with chemical or plasma have been investigated [4–8]. Nevertheless satisfactory understanding in all details such as the frequency dependence of N_{ss} and R_s as function of applied bias voltage has still not been achieved. This fact causes a high level of in-plane stress and threading dislocation density (DD) generation, as grown by metal–organic chemical vapor deposition (MOCVD) in the GaN epitaxial layer [6–8]. Surface preparation, interruption of the periodic lattice structure at the surface, formation of an insulator layer and barrier at metal/semiconductor (M/S) interface and impurity concentration of semiconductor leads to the formation many N_{ss} and DD at M/S interface [9–15]. Moreover, interface preparation process, barrier height, high quality ohmic and Schottky contacts affect the performance of electronic devices [9,10,16–19]. Therefore, these possible sources of error must be taken into account to obtain accurate and reliable results.

Recently, the frequency dependence of the electrical characteristics of these devices has become an object of rather intense interest in the literature [11–25]. However, from experimental and theoretical point-of-view, the satisfactory description of the effect of these parameters on the C–V and G/ω–V characteristics still remains as an important problem. Therefore, the frequency dependent reverse and forward bias C–V and G/ω–V measurements in the wide frequency range can give us important information about the energy distribution of the interface states and the main electrical parameters of these structures.

In the ideal case, the capacitance of these structures is usually frequency independent. However, the situation is different especially in the weak inversion and depletion regions for low frequencies due to the existence of N_{ss} and their relaxation time, formation

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of the barrier height at MS interface and R_s of structure. The interface trapped charges in general called as the interface states exist within the forbidden band gap. These traps can be divided in four categories: (1) interface trap charges (Q_{it}), (2) fixed oxide charges (Q_f), (3) oxide trapped charges (Q_{ot}) and (4) mobile ionic charges (Q_m) such as sodium ions, which are mobile within the oxide under bias-temperature aging conditions. These interface charges can easily follow an ac signal and yield an excess capacitance and conductance to their real values at low frequencies. On the contrary, the charges at interface states can't follow an ac signal and can't produce an excess capacitance and conductance at high frequencies where the carrier life time of the charges (τ) is much larger than $1/f$. Therefore, the frequency dependent C–V and G/ω–V measurements are very significant to obtain accurate and reliable results about these fabricated structures. The interface states usually cause a bias shift and frequency dispersion in the capacitance–voltage (C–V) and conductance-voltage (G/ω–V) curves [12,14,16] and they are effective especially in the depletion and inversion regions.

In addition, the series resistance is also an important parameter, which causes deviations in the electrical characteristics at only depletion region of these structures [9,15,20,21]. The R_s of device can cause a serious error in the I–V, C–V and G/ω–V characteristics. In general, the origins of R_s can arise from five different sources: contact made by the probe wire to the gate; the ohmic and rectifier contacts; the resistance of the quasi-neutral bulk semiconductor between ohmic contact to semiconductor and the depletion layer edge at the semiconductor surface; the oxide charges or organic impurities in the interfacial layer and inhomogeneity of the density distribution of doping material in semiconductor [2]. To avoid these errors and the sensitivity limitation, R_s can be minimized by sample fabrication processes, making measurements at low frequencies so that the effect of R_s is negligible, the measurements carried out in dark and in sheeted box or cryostat and to make desired correction in the experimental measurements.

In order to extract the energy density distribution profile of interface states for these devices, several method have been suggested in the literature such as the high–low frequency capacitance (C_{HF}–C_{LF}) [20,22], quasi-static capacitance [21], surface admittance [15], forward bias current–voltage [18] and conductance techniques. Among them the more important ones are high-low frequency capacitance and conductance techniques [23].

The conductance method, as developed by Nicollian and Goetzberger [16,17], is based on the conductance losses resulting from the exchange of majority carriers between the interface states and the majority carrier band of the semiconductor when a small ac signal is applied to the these structures. The applied ac signal causes the Fermi level to oscillate about the mean positions governed by the dc bias, when the structure is in depletion. Therefore, the conductance technique gives an accurate simultaneous determination for interface states density, their relaxation time (τ) and capture cross section as a function of energy (σ) [16,17,21]. According to this method, the interface states at the Fermi level change their occupancy by capture and emission process, and a conductance loss occurs, since the response of states lags behind the phase of the signal. The density of states is found from the conductance loss resulting from the interface states by measuring the ac conductance as a function of bias voltage in depletion at various frequencies.

In this study, we experimentally investigated the frequency dependence of forward and reverse bias C–V and G/ω–V characteristics of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure in the wide frequency range of 2 kHz −2 MHz by considering both the interface states (N_{ss}) and series resistance (R_s) effects. Also the forward and reverse bias I–V characteristics of these structures were measured at room temperature. The interface states density values at M/S interface were obtained from admittance spectroscopy method.

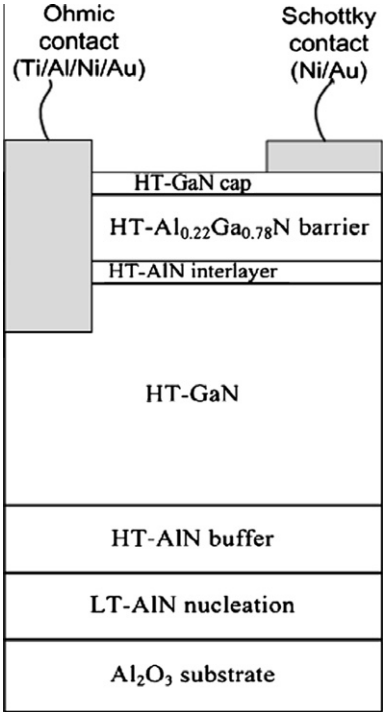

Fig. 1. Schematic diagram of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures and a view of ohmic and Schottky contacts on the structures.

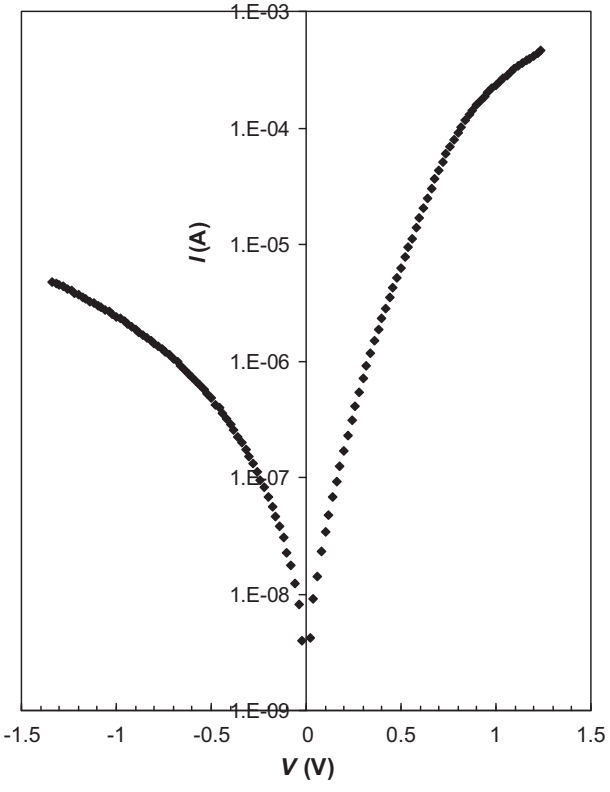

Fig. 2. Forward and reverse bias current–voltage (I–V) characteristics of the Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure in semi-logarithmic scale at room temperature.

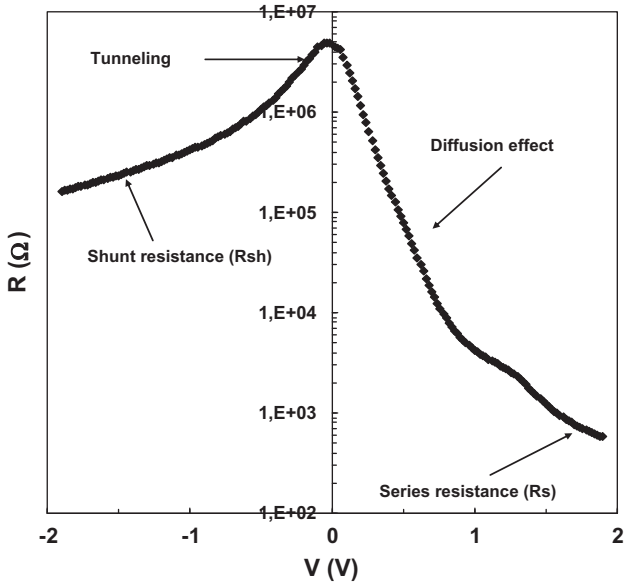

Fig. 3. The variation of R_S as a function of bias voltage for (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure at room temperature.

2. Experimental procedures

The samples investigated in the present study were grown on *C*-face (0 0 0 1) sapphire (Al_2O_3) substrate by a low-pressure MOCVD reactor. Hydrogen was used as the carrier gas and Trimethylgallium (TMGa), trimethylaluminum (TMAl), ammonia (NH_3) were used as Ga, Al and N precursors, respectively. Prior to the epitaxial growth, the substrate was cleaned in H_2 ambient at 1100 °C. As shown in Fig. 1 , 15 nm low-temperature (LT) AlN nucleation layer was grown at 840 °C with a 50 mbar reactor pressure. After the deposition of the LT-AlN nucleation layer, the wafers were heated to a high temperature (HT) for annealing. For the samples, approximately a 0.60 μm HT–AlN buffer layer was deposited on the annealed nucleation layers at 1127 °C with a 400 nm/hr growth rate. After the deposition of buffer layers, approximately 1.9 μm HT–GaN layer was grown at 1040 °C. Finally, 1.5 nm thick AlN interlayer, a 27 nm thick $Al_{0.22}Ga_{0.78}N$ barrier layer, and 3 nm GaN cap layer were grown at 1080 °C. All layers are nominally undoped.

For the contacts, since the sapphire substrate is insulating, the ohmic and Schottky contacts were made on the top surface. The ohmic contacts were prepared by the evaporation deposition of Ti/Al/Ni/Au (200 Å/2000 Å/300 Å/700 Å). After the metallization step, the contacts were annealed at 850 °C for 30s in N_2 ambient in order to form the ohmic contact. The Schottky contacts were prepared by the evaporation deposition of Ni/Au (300 Å/500 Å). Both ohmic and Schottky contacts were made on the top surface as 1.5 mm-diameter circular dots.

The current–voltage (*I–V*) characteristics were performed by the use of a Keithley 220 programmable constant current source, a Keithley 614 electrometer. The capacitance–voltage (*C–V*) and conductance-voltage (G/ω–*V*) characteristics were measured in the 2 kHz–2 MHz frequency range, using a HP 4192 A LF impedance analyzer (5 Hz–13 MHz) and test signal of 40 mVrms. All of the measurements were carried out with a temperature controlled Janes vpf-75 cryostat.

3. Results and discussion

3.1. The voltage dependent forward bias I–V characteristics

Fig. 2 shows the semi-logarithmic forward and reverses bias *I–V* characteristics of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure at room temperature. The current voltage characteristics of the metal–semiconductor contacts (diodes) with a series resistance (R_s) can be analyzed by the following relation [9]

$$I = I_o \exp\left(\frac{q(V - IR_s)}{nkT}\right)\left[1 - \exp\left(\frac{-qV - IR_s}{kT}\right)\right] \quad (1)$$

where *n* is the ideality factor can be obtained from the slope of the straight line region of the ln(*I*)–*V* plot, *k* is the Boltzmann constant, R_s is the series resistance of the structure, *V* is the applied bias voltage, *T* is the sample temperature in Kelvin. Here, I_o is the reverse

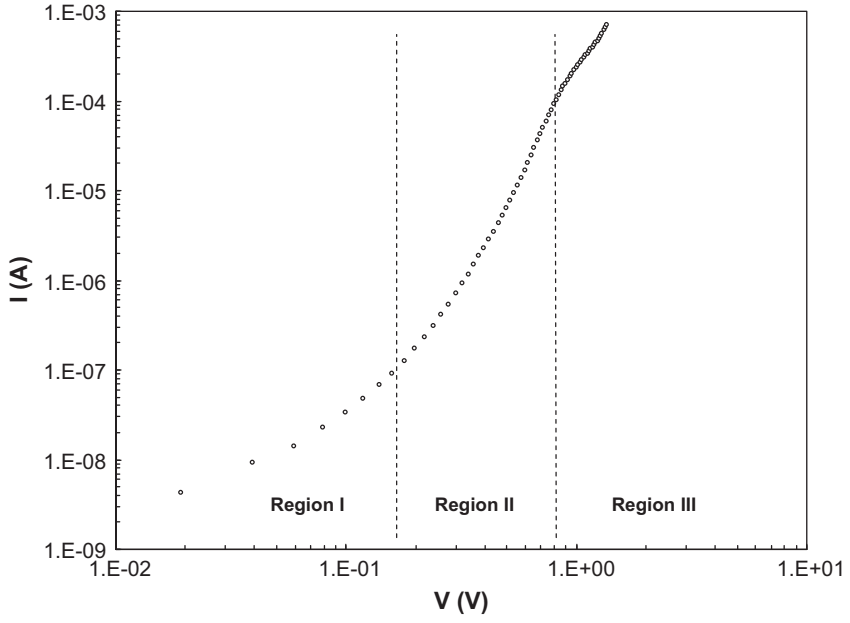

Fig. 4. The ln(*I*) vs. ln(*V*) characteristics of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure at room temperature.

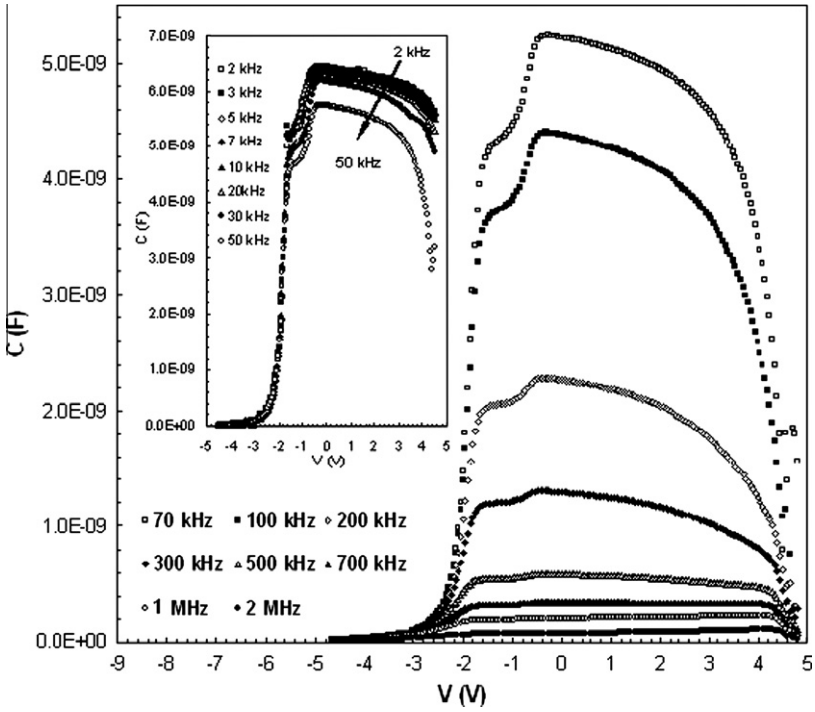

Fig. 5. The frequency dependent curves of the C–V characteristics of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure at room temperature.

saturation current derived from the straight line region of the forward bias current intercept at zero bias and is given by

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{Bo}}{kT}\right) \quad (2)$$

Thus, the ideality factor (n) and zero bias barrier height (Φ_{Bo}) of structure were determined from Eqs. (1) and (2) as 2.36 and 0.74 eV, respectively. The high value of n was attributed to the high density of interface states localized at MS interface and the effect of barrier inhomogeneities [9,19]. As shown in Fig. 2, the presence of high R_S causes the downward concave curvature in the forward bias I–V plot at high bias voltages. The voltage dependent R_S profile of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure at room temperature was obtained from the I–V data by using Ohm's law ($R_i = V_i/I_i$) and is given in Fig. 3. The R_S and shunt resistance (R_{sh}) values of structure were calculated from the R–V plot as 0.578 k Ω and 166.13 k Ω, respectively. It is clear that the structure has low series resistance and high shunt resistance which actually is necessary for ideal devices. As shown in Fig. 3, the value of R_S gives a peak which can be explained by the effect of tunneling in the current conduction mechanism.

In order to detect the dominant current conduction mechanism, I–V characteristics of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure was drawn also in logarithmic scale in Fig. 4. As can be seen in the figure, the forward bias current plot reveals three distinct regions: a linear region below "0.22 V", an excess current or "hump" at about "0.22 V"–"0.82 V", and a deviation from the ln(I) vs. V relationship above "0.82 V". Similar results have been reported in the literature [24–27]. Also, the non-saturation behavior was observed (Fig. 2) as a function of bias in the experimental reverse bias range. This behavior may be explained in terms of the spatial inhomogeneity of Schottky barrier height (SBH) [28,29], and the image force lowering effect of SBH [13,30].

In region I, the simple thermionic emission (TE) theory can be used to obtain main electrical properties of the structure. In region II, the forward bias I–V characteristics as shown in Fig. 2 exhibit a "hump". Kar and Dahlke [14] have shown that "humps" in the forward current–voltage characteristics of MIS diodes originate from carrier generation-recombination at interface states and subsequent tunneling through the oxide to the metal. In region III, the forward I–V plot deviates from the relationship given by Eq. (1). The current through the diode appears to become limited by another process. The absolute

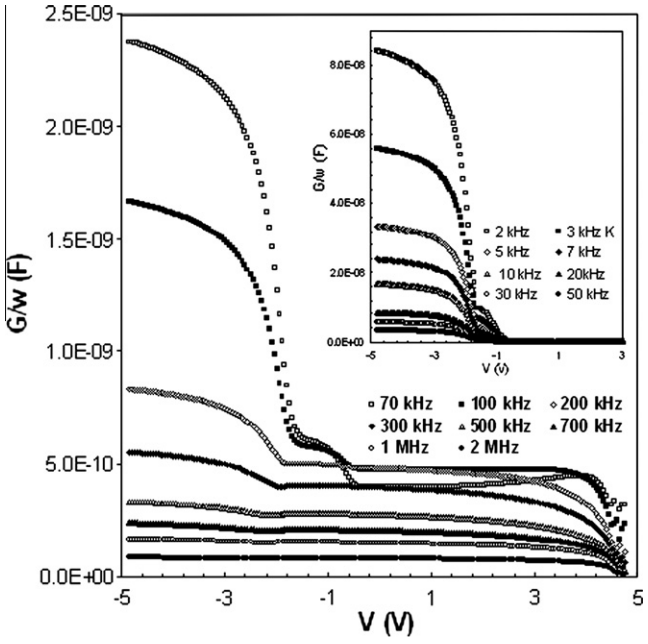

Fig. 6. The frequency dependent of G/ω–V characteristics for (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure at room temperature.

current values reveal that this limitation is not due to the series resistance of the bulk silicon or the ohmic contact. The most likely explanation is that, above "0.82 V", the current is determined by transport across the interfacial oxide layer. Possible conduction processes include quantum mechanical tunneling and Poole–Frenkel conduction via impurity states. Also in this region the injection of charge carriers takes place and causes an increase in the current.

3.2. The frequency dependent forward and reverse bias C–V and G/ω–V characteristics

The forward and reverse bias *C–V* and *G/ω–V* measurements were performed at room temperature in the frequency range of 2 kHz–2 MHz by using HP 4192A LF impedance analyzer and are given in Figs. 5 and 6, respectively. As shown in Fig. 5, *C–V* curves vary from the weak inversion region to strong accumulation region

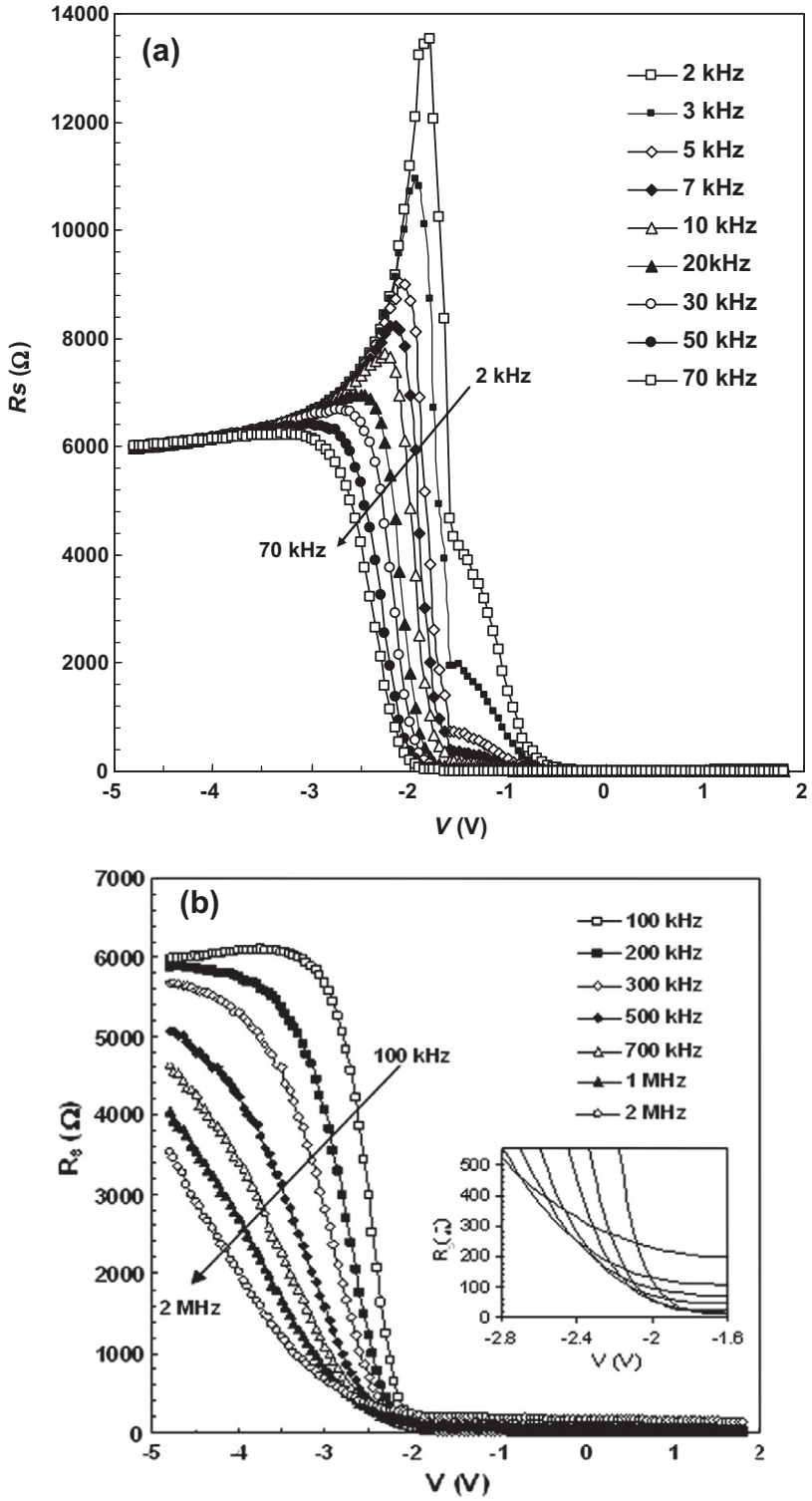

Fig. 7. R_s–*V* characteristics of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure (a) at low frequencies (b) at high frequencies.

for each frequency. The high values of C and G/ω at low frequencies are due to the excess capacitance which is resulting from the interface states localized at M/S interface. If the C–V measurements are carried out at sufficiently low frequencies (such that the carrier lifetime (τ) of charge at trap is much lower than the reverse of angular frequency ($1/2f$), the N_{SS} will easily follow an ac signal and yield an excess capacitance and conductance to their measurement values [16,17].

However, at higher frequencies, the N_{SS} cannot follow the ac signal and in this case, the contribution of interface states capacitance (C_{ss}) and conductance (G_{ss}/ω) to the total measured capacitance (C_m) and conductance (G_m/ω) negligibly small [16,17,31,32]. At high frequencies, the R_s become significant because of the low impedance of the device. In addition, the C–V characteristics of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure shows two peaks. The first peak located at low forward bias (in depletion region) due to N_{ss} contribution shifts towards the low bias voltages with the increasing frequency. However, the second peak shown at high bias region disappears (due to the influence of the R_s) when the frequency decreases [33].

There are several methods in literature for determining R_s values [17,34,35]. We have applied the admittance method developed by Nicollian and Brews [17]. This method provides the determination of R_s in both reverse and forward bias regions. According to this method, the real value of R_s for MIS or MOS structures can be subtracted from the measured C_m and G_m values at sufficiently high frequencies ($f \geqslant 500$ kHz) and in strong accumulation regions as following [17]

$$R_s = \frac{G_m}{G_m^2 + (\omega C_m)^2} \tag{3}$$

where, ω (=$2\pi f$) is the angular frequency. The voltage dependent R_s values were calculated according to Eq. (3) and shown in Fig. 7a and b for low and high frequencies, respectively. These very significant values demanded that special attention should be given to effects of the R_s in the application of the admittance-based measurement methods (C–V and G/ω–V). As seen in Fig. 7a and b, the R_s–V plots give a peak especially at low frequencies between about (−2)–(−1) V depending on frequency such that the peak disappears at high frequencies.

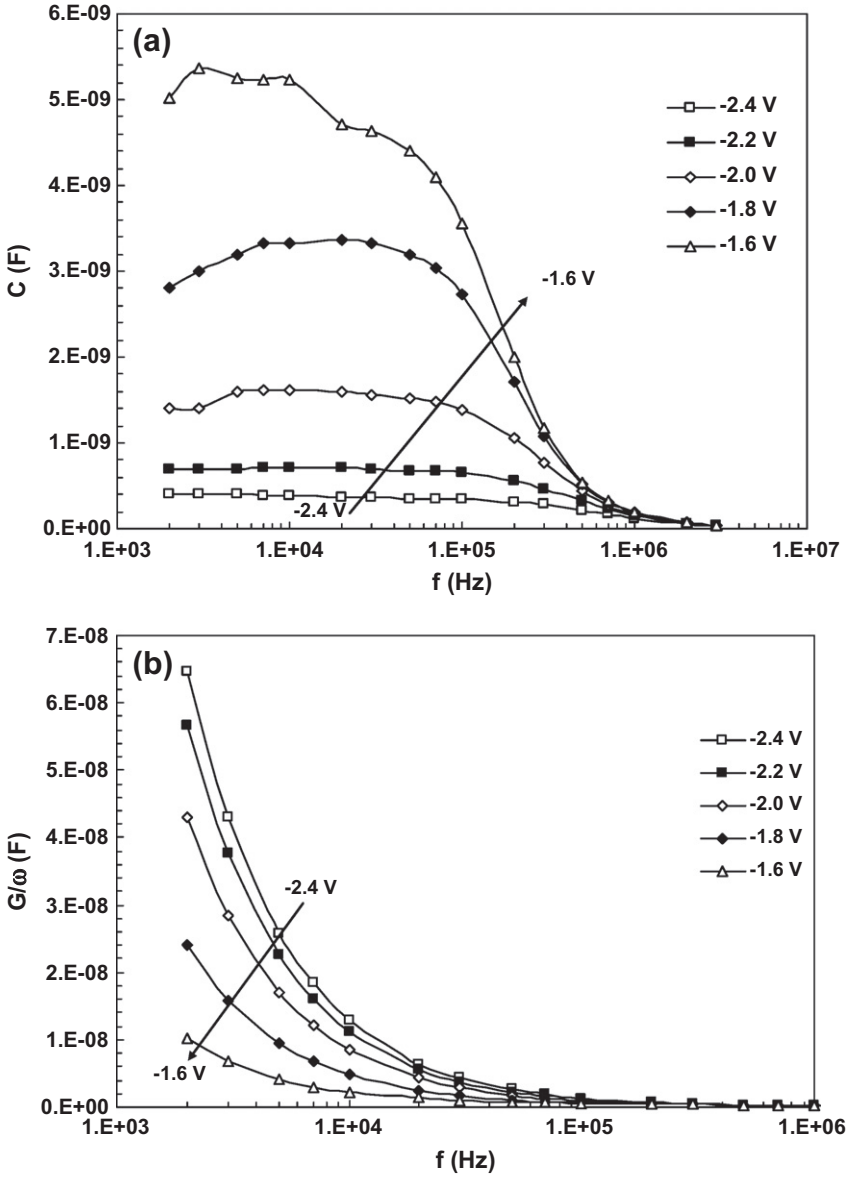

Fig. 8. The frequency dependence of: (a) the $C(V_G)$-f and (b) $G/\omega(V_G)$-f characteristics of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure at room temperature.

In order to obtain the real values of C and G/ω for the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures, the high frequencies measured capacitance (C_m) and conductance (G_m/ω) as measured under forward and reverse bias voltages were corrected for the effect of R_s [17]. It can be seen from Fig. 7, the R_s values are dependent on both frequency and applied bias voltage and they change from region to region due to special distribution of interface states at M/S interface. Also, at low frequencies, the carrier lifetime (τ) in these traps is much lower than the reverse of angular frequency ($1/2\pi f$), hence they can easily follow an ac signal and yield an excess capacitance and conductance to their measurement values [16,17].

In order to clarify the observed behavior of measured C_m and G_m/ω in Figs. 5 and 6, we obtained the C_m and G_m/ω values of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure as a function of frequency for five gate voltages and are given in Fig. 8a and b, respectively. As can be seen in these figures, both the C_m and G_m/ω values almost decrease with the increasing frequency in the frequency range of 2 kHz–2 MHz. This behavior can be attributed to the existence of a continuous distribution of N_{ss} in the M/S interface, which leads to a progressive decrease in the response of the N_{ss} to the applied ac voltage [36–38]. On the other hand, it is well known that at low frequencies the charges at interface states can easily follow an external ac signal and yield excess capacitance and conductance especially in the depletion and weak inversion regions. As can be seen in Fig. 8a, "−1.6", "−1.8", and "−2.0 V" values corresponding to depletion region. On the other hand, "−2.2 V" and "−2.4 V" corresponds to inversion region. Also, while the interface states are especially effective in depletion region but series resistance is effective only at accumulation region. The other explanation of such behavior can be attributed to the particular distribution of interface states located at M/S interface with energy states in the semiconductor forbidden band gap. In addition, the higher value of C and G/ω at low frequency are due to the excess capacitance (C_{ex}) and conductance (G_{ex}/ω) resulting from the N_{ss} in equilibrium with the semiconductor that can follow the ac signal. As a result, in the depletion region the N_{ss} are responsible for the observed frequency dispersion in C (V_G) and $G/\omega(V_G)$ plots.

The conductance of interface states G_{ss} as a function of frequency of the applied signal proposed by Nicollian and Brews is given by [17]

$$G_{SS} = \frac{C_{ox}^2 G}{(C_{ox} - C)^2 + (G/\omega)^2} \tag{4}$$

where C and G/ω are the experimental capacitance and conductance of the heterostructure, respectively. As explained in Refs. [16,17,38–41], the conductance method yields more accurate and reliable results. Fig. 9 depicts the G_{ss} vs. log (f) plot for five gate voltages which show a maximum with the increasing bias, and the amplitude of the peak $(G_{ss})_{max}$ decreases with the frequency (ω_p) at which the occurred maxima moves towards lower value. This behavior can be explained by using the interface trap model. As indicated before, there exists an almost continuous distribution of N_{ss} energy levels. At a given bias, the Fermi energy level (E_F) fixes the occupancy of these trap levels and a particular electron density will exist at M/S interface which determines the capture rate of the related trap levels. Capture and emission occurs primarily by traps located within a few kT/q above and below the E_F. If the frequency is slightly different from the capture rate, losses are reduced because trap levels either do not respond or the response occurs at a different frequency. Therefore, the loss peak is a function of frequency. Furthermore, the peak value depends on capture rate, i.e., on the interface trap level occupancy, which is determined by the applied gate bias voltage [42,43].

The energy position in the band gap of semiconductor can be calculated as

$$E_C - E_{SS} = q(\Phi_S - \Phi_F) \tag{5}$$

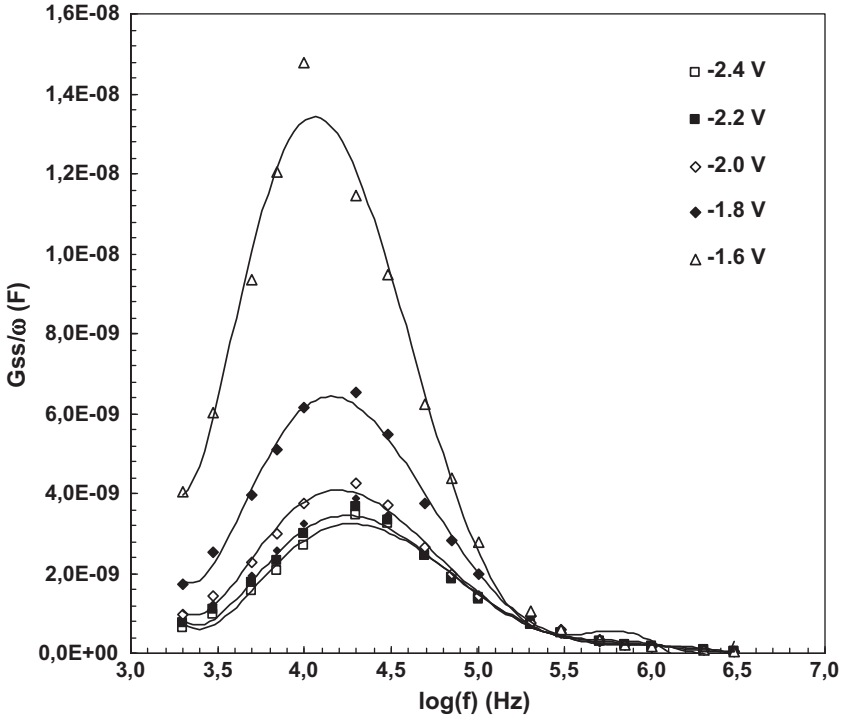

Fig. 9. The frequency dependence of Gss characteristics obtained from the experimental forward bias capacitance and conductance measurements of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure at room temperature.

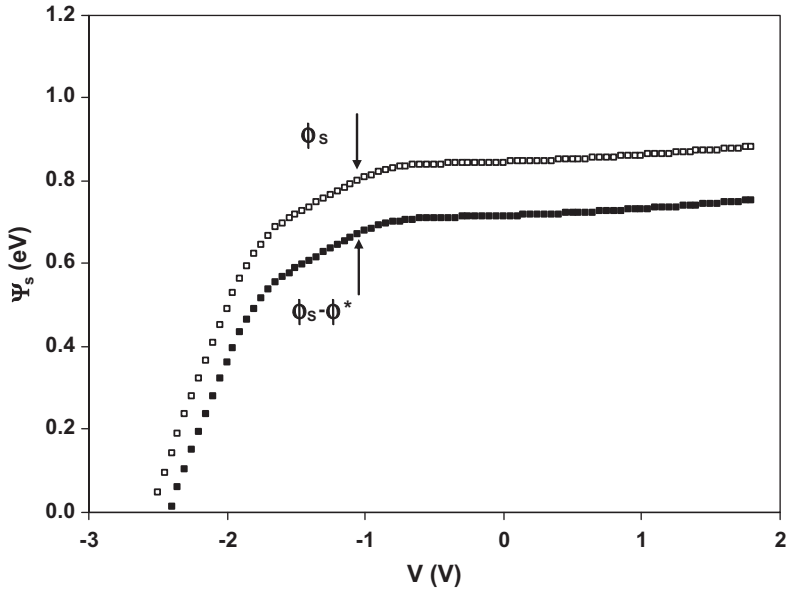

Fig. 10. The surface potential vs. *V* plot of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure at room temperature.

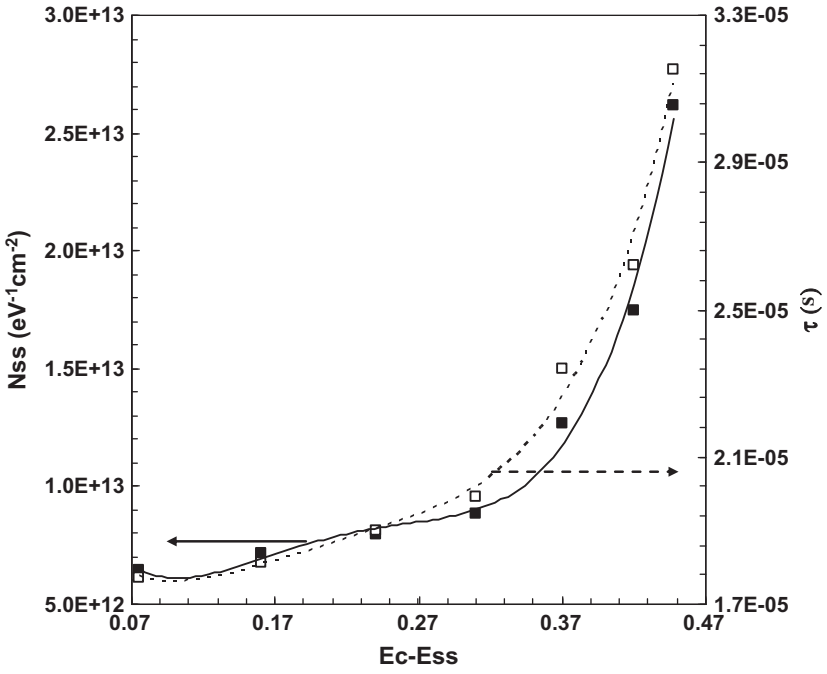

Fig. 11. The energy distribution of interface states and their time constant obtained from conductance method for (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures at room temperature.

where Φ_F is the position of Fermi energy level $\Phi_F = kT/q\ \ln(N_C/N_D)$. The surface potential (Φ_s) as a function of bias is found from the numerical integration of the lowest measureable frequency *C–V* curve according to

$$\Phi_S = \int_{V_a}^{V_i} [1 - C_{LF}/C_{ox}]dV_G + \Phi^* \quad (6)$$

where V_a is the bias voltage in strong accumulation when the capacitance is equal to the oxide capacitance C_{ox} and the integration constant Φ^* was found by extrapolation of the $C_{sc}^{-2} - \Phi_S$ curve in the depletion region (0.13 eV) to $C_{sc}^{-2} = 0$ [17,44]. The surface potential vs. applied voltage is shown in Fig. 10. The energy position is calculated by the Eq. (5). From the slope of the C^{-2} vs. *V* plot in the inversion region at 2 MHz, the doping density N_D of the substrate is determined to be 2.48×10^{14} cm^{-3}. As can be seen in Fig. 9 for each gate bias the G_{ss}–ln(*f*) plot shows a peak, and due to the N_{ss} contribution the peak position shifts from low frequency to high as the bias changes from depletion toward the accumulation region as predict by the theory. Each plot goes through a maxima at $\omega\tau = 1.98$ with values of $(G_{ss})_{max} = 0.402\ qA\ N_{ss}$. The ordinates and frequencies of the maxima yield density of the N_{ss} and their time constant "τ", respectively. The values of the interface states and their relaxation time are shown in Fig. 11. It is observed that both interface state density N_{ss} and their time constant τ show decrease

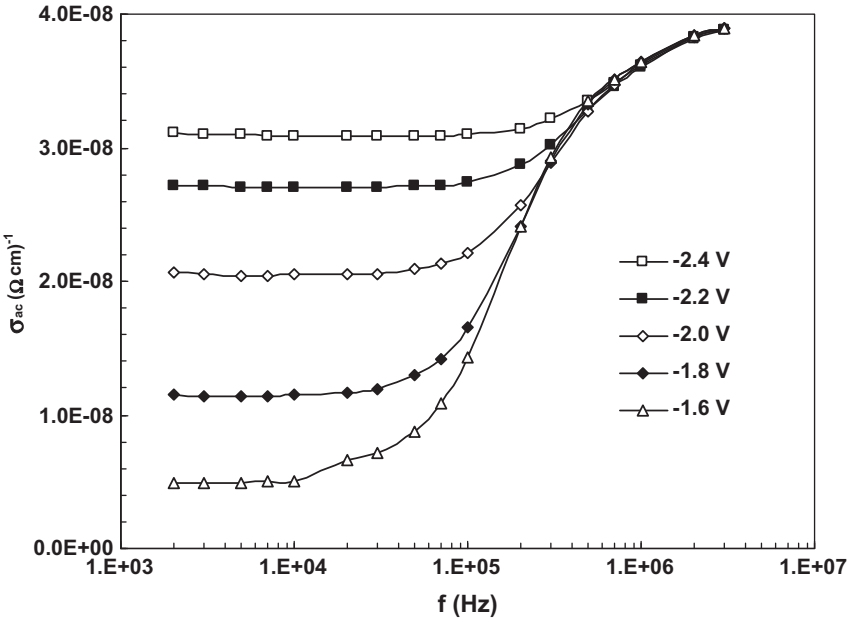

Fig. 12. Frequency dependence of ac electric conductivity (σ_{ac}) for various applied voltage of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures at room temperature.

with the increasing energy from the bottom of the conduction band. As can be seen in Fig. 11, the values of N_{ss} rise exponentially with bias (or E_{ss}) without any peak and minimum. On the other hand, Aydın et al. [40] found that density distribution profile of N_{ss} has U shape behavior. Similar results have been also reported in literature [45,46]. Such behavior of N_{ss} can be attributed to interface state continuum and not with single level states or bands of interfacial states as suggested by Kar and Dahlke [14]. The other explanation of such behavior may be the particular distribution of interface states where the charges located at the semiconductor/interfacial layer interface with energy states in the semiconductor forbidden band gap. In other word, the energy density distribution of N_{ss} profile depends on many factors such as frequency, the magnitude of external ac signal, applied dc voltage, the interfacial layer deposited or native, the fabrication process, the life time of charges at interface states and the homogeneity of interfacial layer. Therefore, the energy density distribution profile of N_{ss} may show changes from one sample to another.

The behavior of ac electrical conductivity (σ_{ac}) of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure at various voltages is presented in Fig. 12. It is noticed that the electrical conductivity generally increases with the increasing frequency. At low frequency, it is independent of frequency for each voltage. This behavior can be attributed to a gradual decrease in series resistance with increasing frequency [47].

4. Conclusions

The effects of N_{ss} and R_s on the non-ideal electrical characteristics of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures have been investigated by using I–V, C–V and G/ω–V measurements at room temperature. The presence of high values of R_s leads to the downward concave curvature in the forward bias I–V and a peak in C–V characteristics at sufficiently high bias voltage. Experimental values of C and G/ω show large frequency and bias voltage dispersion due to the presence of N_{ss} at MS interface and R_s. It is clear that the three regimes of accumulation, depletion and inversion are clearly shown for each C–V curve. Also, C–V curves have two distinctive peaks which are known to be related with depletion region (first peak) due to N_{ss} contribution and accumulation region (second peak) due to the influence of R_s. The magnitude of these peaks was found to depend strongly on the values of R_s, N_{ss} and the external ac signal superimposed on the dc bias. The ac electrical conductivity (σ_{ac}) values for various bias voltages are almost independent of frequency up to 100 kHz, and after this frequency level they it increase with the increasing frequency. In addition, the high-frequency capacitance (C_m) and conductance (G_m/ω) values measured under forward and reverse bias were corrected to minimize the effect of series resistance. The results indicate that the interfacial polarization can occur more easily especially at low frequencies. Experimental results confirmed that the N_{ss} and R_s are important parameters which influence the electrical characteristics of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures. Therefore, especially the measured C and G/ω must be corrected to eliminate the effect of R_s.

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