Thin Solid Films 548 (2013) 411–418

Contents lists available at ScienceDirect

Thin Solid Films

journal homepage: www.elsevier.com/locate/tsf

Current-Transport Mechanisms in the AlInN/AlN/GaN single-channel and AlInN/AlN/GaN/AlN/GaN double-channel heterostructures

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ARTICLE INFO

Article history:
Received 11 October 2012
Received in revised form 9 September 2013
Accepted 10 September 2013
Available online 17 September 2013

Keywords:
AlInN/AlN/GaN single channel heterostructures
AlInN/AlN/GaN/AlN/GaN double channel heterostructures
Tunneling current
Schottky contact

ABSTRACT

Current-transport mechanisms were investigated in Schottky contacts on AlInN/AlN/GaN single channel (SC) and AlInN/AlN/GaN/AlN/GaN double channel (DC) heterostructures. A simple model was adapted to the current-transport mechanisms in DC heterostructure. In this model, two Schottky diodes are in series: one is a metal–semiconductor barrier layer (AlInN) Schottky diode and the other is an equivalent Schottky diode, which is due to the heterojunction between the AlN and GaN layer. Capacitance–voltage studies show the formation of a two-dimensional electron gas at the AlN/GaN interface in the SC and the first AlN/GaN interface from the substrate direction in the DC. In order to determine the current mechanisms for SC and DC heterostructures, we fit the analytical expressions given for the tunneling current to the experimental current–voltage data over a wide range of applied biases as well as at different temperatures. We observed a weak temperature dependence of the saturation current and a fairly small dependence on the temperature of the tunneling parameters in this temperature range. At both a low and medium forward-bias voltage values for Schottky contacts on AlInN/AlN/GaN/AlN/GaN DC and AlInN/AlN/GaN SC heterostructures, the data are consistent with electron tunneling to deep levels in the vicinity of mixed/screw dislocations in the temperature range of 80–420 K.

1. Introduction

Recently, the lattice-matched AlInN/GaN material system has become of interest for electronic applications due to its promising electronic properties, polarization effects, and high thermal stability [1–5]. The higher polarization-induced two-dimensional electron gas (2DEG) density in the AlInN/GaN high electron mobility transistors (HEMTs) shows superior performance compared to the AlGaN/GaN HEMTs [1–5], which is not only because of the formation of a high density 2DEG at the AlInN/GaN interface, but also because of the possibility to grow lattice matched $Al_{1-x}In_xN$ epitaxial layers with GaN at an indium content x of approx. 17% [4,5]. At the lattice-matched $Al_{0.83}In_{0.17}N$/GaN heterostructure, the interface minimizes strain and thereby cracking and/or dislocation formation [4,5].

The GaN based HEMT structures are usually grown on highly lattice-mismatched substrates, such as sapphire (Al_2O_3) [4], SiC, or Si [6]. The large lattice mismatch and large difference in the thermal expansion coefficients between the GaN layer and the substrates reduce the crystal quality of the GaN epitaxial layer [6]. This fact causes a high level of in-plane stress and threading dislocation generation in the GaN epitaxial layer during growth by metal-organic chemical vapor deposition (MOCVD) [4–6]. The high densities of threading dislocations in the epitaxial layers affect the performance reliability of the device. If many defects exist near the surface region, the electrons can easily go through the barrier by defect-assisted tunneling, thereby greatly enhancing the tunneling probability [7–15].

The current-transport mechanism in these devices, such as metal–semiconductor (MS), metal–insulator–semiconductor, light emitting diodes (LEDs), and solar cells, is dependent on various parameters, such as the process of surface preparation, formation of an insulator layer between the metal and semiconductor, Schottky barrier height (SBH) inhomogeneity, impurity concentration of a semiconductor, density of interface states, defects, or dislocations, series resistance (R_s) of a device, device temperature, and bias voltage. In these devices, a number of carrier transport mechanisms, such as quantum mechanical tunneling, thermionic-emission (TE), thermionic-field-emission, minority carrier injection, recombination–generation, and multi-step tunneling, compete and usually one of them may dominate over the others at a certain temperature and in certain voltage regions [7]. Several investigations have been reported to analyze the dominant current-transport mechanism in GaN-based Schottky diodes. Tunneling current and thermionic field emission are both considered as dominant current transport mechanisms [8–20]. Evstropov et al. [8,10] and Balyaev et al. [13] showed that the current flow in the III–V heterojunctions is generally governed by multistep tunneling with the involvement of dislocations even at room temperature. They demonstrated that an excess tunnel current can be attributed to dislocations. A model of tunneling through a space charge region along a dislocation line (tube) is suggested [8,10,13–15]. The unrealistically

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http://dx.doi.org/10.1016/j.tsf.2013.09.026

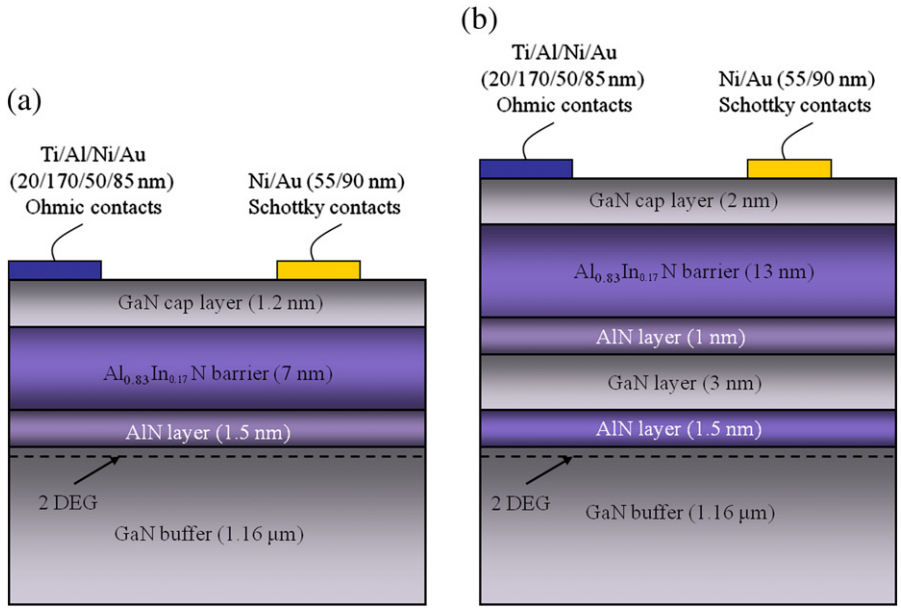

Fig. 1. Schematic illustration of (a) AlInN/AlN/GaN SC and (b) AlInN/AlN/GaN/AlN/GaN DC heterostructures.

large ideality factors obtained from the current–voltage (*I–V*) characteristics over a wide range of forward bias for LEDs were explained by tunneling current mechanisms [16–20].

Analysis of the forward bias *I–V* characteristics at a wide temperature range enables us to understand the different aspects of the current-conduction mechanism and barrier formation. Chen et al. [20] used a simple model to describe the gate current–voltage characteristics of the modulation-doped field effect transistor (MODFET's) and heterostructure insulated-gate field-effect transistors (HIGFET). Their model consists of two Schottky diodes in series: one is a metal–semiconductor (AlGaAs) Schottky diode and the other is an equivalent Schottky diode due to the heterojunction between the AlGaAs and GaAs [20].

The main aim of the present study is to investigate the current-conduction mechanisms in the Schottky contacts on AlInN/AlN/GaN single channel (SC) and AlInN/AlN/GaN/AlN/GaN double channel (DC) heterostructures with a high dislocation density compared with the literature over a wide temperature range (80–420 K). We adapted this model, which was used by Chen et al. [16], to AlInN/AlN/GaN SC and DC heterostructures. In order to describe the *I–V* characteristics in SC heterostructure, an equivalent Schottky diode, due to the heterojunction between the metal–semiconductor (AlInN) was used, but in the DC, we used two equivalent Schottky diodes in series: one is a metal–semiconductor (AlInN) Schottky diode and the other is an equivalent Schottky diode due to the heterojunction between the AlN and GaN.

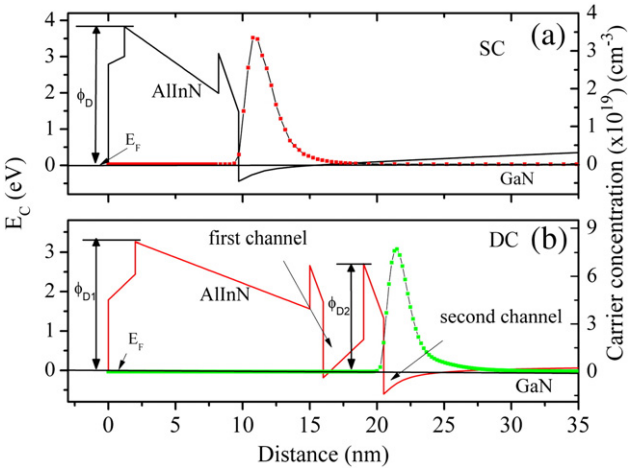

Fig. 2. Calculated band profile and 2DEG distribution along the z axis for Schottky contacts on (a) AlInN/AlN/GaN SC and (b) the AlInN/AlN/GaN/AlN/GaN DC heterostructures.

2. Experimental procedure

The $Al_{1-x}In_xN$/AlN/GaN (x ≅ 0.17) SC and $Al_{1-x}In_xN$/AlN/GaN/AlN/GaN (x ≅ 0.17) DC heterostructures were grown on double-polished 2-inch diameter c-face Al_2O_3 substrates in a low pressure MOCVD reactor (Aixtron 200/4 HT-S) by using trimethylgallium, trimethylaluminum, trimethylindium and ammonia as Ga, Al, In and N precursors, respectively. Prior to the epitaxial growth, the Al_2O_3 substrate was annealed at 1100 °C and at a reactor pressure of 2×10^4 Pa for 10 min in order to remove surface contamination. The buffer structures consisted of a 15 nm thick, low-temperature (770 °C) AlN nucleation layer, and high temperature (1120 °C) 270 nm AlN template layer. A 1.16 μm thick nominally undoped GaN layer was grown on an AlN template layer at 1060 °C, followed by a 1.5 nm thick high temperature AlN (1075 °C) spike layer. The AlN barrier layer was used to reduce the alloy disorder scattering by minimizing the wave function penetration from the 2DEG channel into the AlInN layer. After the deposition of these layers, a 7 nm thick undoped $Al_{0.83}In_{0.17}N$ barrier layer was grown at 830 °C. Finally, a 1.2-nm-thick GaN cap layer growth was carried out at a temperature of 830 °C (Fig. 1(a)). In the DC heterostructure,

Table 1
Lattice parameters (*a* and *c*), piezoelectric constants (e_{31} and e_{33}), elastic constants (C_{13} and C_{33}), diecetric constant (ε_{11} and ε_{33}) and spontaneous polarization (P_{SP}) values of wurtzite AlN, GaN, InN materials [22].

Wurtzite	AlN	GaN	InN
a (nm)	0.3112	0.3189	0.3545
c (nm)	0.4982	0.5185	0.5705
$e_{31}(C/m^2)$	−0.60	−0.49	−0.57
$e_{33}(C/m^2)$	1.46	0.73	0.97
ε_{11}	9.0	9.5	–
ε_{33}	10.7	10.4	14.6
C_{13} (GPa)	108	103	92
C_{33} (GPa)	373	405	224
$P_{SP}(C/m^2)$	−0.081	−0.029	−0.032

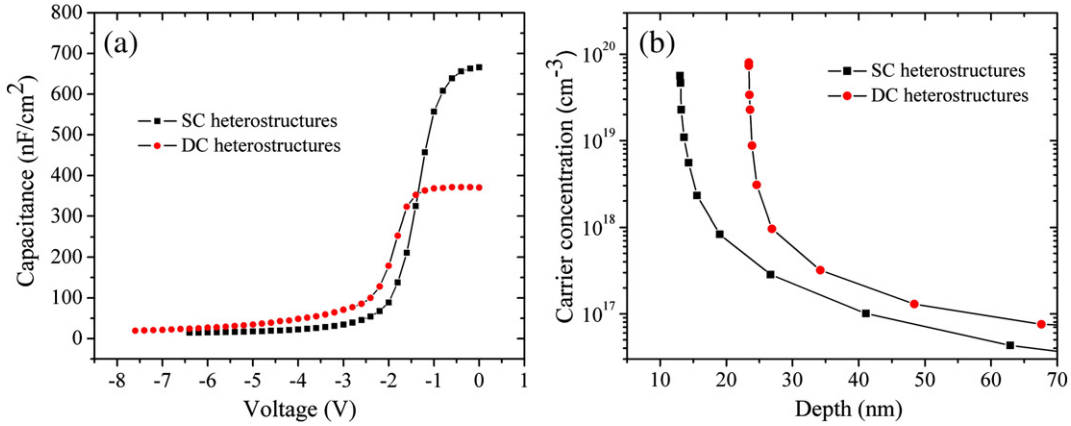

Fig. 3. (a) Measured *C–V* characteristics of the single and double channel heterostructures. (b) The carrier density depth profiles calculated from *C–V* measurements. The onset of the 2DEG is 10.7 and 21.5 nm for Schottky contacts on SC and DC heterostructures, respectively.

we used 1 nm AlN (1075 °C) and 3 nm GaN (1075 °C) between the $Al_{0.83}In_{0.17}N$ barrier layer and the AlN spike layer. The thickness of the $Al_{0.83}In_{0.17}N$ barrier layer, grown at 830 °C in the DC heterostructure, is 13 nm. Finally, a 2 nm GaN nm-thick GaN cap layer growth was carried out at a temperature of 830 °C in DC heterostructure (Fig. 1(b)).

Prior to ohmic contact formation, the samples were cleaned with acetone in an ultrasonic bath. After acetone cleaning, the samples were treated with boiling isopropyl alcohol for 5 min and rinsed in deionized water with 18 M Ω resistivity. Then, the samples were dipped in a solution of HCl/H_2O (1:2) for 30 s in order to remove the surface oxides, and rinsed in DI water again for a prolonged period. After cleaning, the ohmic contacts were formed as a square van der Pauw shape and the Schottky contacts formed as 0.8 mm diameter circular dots by using electron beam evaporation at approx. 1.33×10^{-5} Pa vacuum values. The Ti/Al/Ni/Au (20/170/50/85 nm) metals were thermally evaporated on the sample and were annealed at 650 °C for 30 s in N_2 ambient in order to form the ohmic contact. Schottky contacts were formed by Ni/Au (55/90 nm) evaporation. Room temperature Hall measurements were carried out by using van der Pauw geometry at 0.5 T magnetic fields. The measured Hall mobilities and the sheet electron densities are 1482 cm^2/Vs and 1374 cm^2/Vs, 5.2×10^{12} and 1.8×10^{13} cm^{-2} for SC and DC heterostructures, respectively.

The temperature dependence of the current–voltage measurements of the SC and DC heterostructures was obtained in the range of 80–420 K by using a temperature controlled MMR VTHS cryostat, which enables us to make measurements in the temperature range of 80–580 K. The sample temperature was continually monitored by using a copper–constantan thermocouple close to the sample, and the *I–V* measurements were performed with a Keithley model 6517A Electrometer/High Resistance Meter. The capacitance–voltage (*C–V*) measurements were carried out by using an Agilent B1500A semiconductor device analyzer and an Agilent E4980A LCR meter with a test signal of 1 MHz frequency and 40 mV peak to peak AC bias voltages at room temperature.

3. Results and discussion

The conduction potential band profiles and the carrier concentration in pseudomorphic AlInN/AlN/GaN SC and AlInN/AlN/GaN/AlN/GaN DC heterostructures were calculated by solving one-dimensional nonlinear Schrödinger–Poisson equations, self-consistently including polarization induced carriers [21]. Fig. 2 shows the conduction band profiles and the spatial distribution of the carrier concentrations. The material parameters of AlN, GaN, and InN that were used in the calculations are taken from several references given in Table 1 [22]. The material parameters of AlInN for simulation were deduced using Vegard's law and the layers were assumed to be pseudomorphically grown. The spatial distributions of the electrons in the SC/DC AlInN/GaN heterostructures are given in Fig. 1. In the SC heterostructure, the electrons were confined in one electron channel near the AlN/GaN interface. However, in the AlInN/AlN/GaN/AlN/GaN DC heterostructure, the carriers were confined in the second channel with a very small amount of the electrons in the first channel compared with the second channel, as seen in Fig. 2(a) and (b). The calculated electron peak density corresponds to the location of the 2DEG channel at the SC in InAlN/GaN interface, which is ≈10.7 nm below the surface (in Fig. 2 the surface is taken at $x = 0$) and, for the DC sample, the electron peak density is at the AlN/GaN interface and ≈21.5 nm below the surface. The electron concentration peak values are approx. on the order of $\approx 3.3 \times 10^{19}$ cm^{-3}

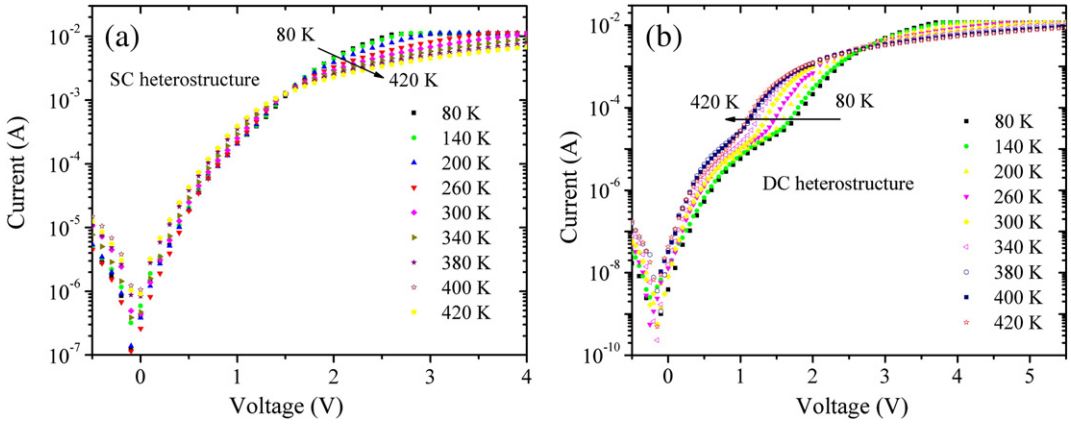

Fig. 4. Measured forward bias current–voltage characteristics of Schottky contacts on (a) AlInN/AlN/GaN SC and (b) AlInN/AlN/GaN/AlN/GaN DC heterostructures at different temperatures.

Table 2
Temperature dependent values of the ideality factor (n), tunneling saturation current (I_{t0}), tunneling parameters (E_0)for SC heterostructure and ideality factor (n_1), tunneling saturation current (I_{t01}) and tunneling parameters (E_{0D1}) for diode 1, ideality factor (n_1), tunneling saturation current (I_{t01}) and tunneling parameters (E_{0D1}) for diode 2, determined from the forward bias I–V characteristics of SC and DC heterostructures, respectively, by least-squares fit of tunneling current mechanism (Eq. (5)) to measured I–V data, are listed.

	SC heterostructure			DC heterostructure					
				Diode 1			Diode 2		
T (K)	n	$I_{t0} \times 10^{-6}$(A)	E_0 (eV)	n_1	$I_{t01} \times 10^{-8}$(A)	E_{0D1} (eV)	n_2	$I_{t02} \times 10^{-9}$(A)	E_{0D2} (eV)
80	20.0	1.3	0.194	14.8	1.6	0.145	29.6	5.0	0.186
140	12.6	1.6	0.193	10.7	2.3	0.143	16.7	5.8	0.186
200	7.9	1.4	0.187	6.4	2.8	0.138	10.5	6.8	0.175
260	5.6	0.9	0.177	4.7	2.9	0.125	7.5	8.0	0.165
300	5.1	1.5	0.181	3.8	3.6	0.124	6.2	20.0	0.161
340	4.5	1.7	0.170	3.5	4.0	0.121	5.2	42.0	0.160
380	4.4	2.0	0.164	3.2	9.8	0.120	6.1	78.2	0.161
400	4.2	2.1	0.162	3.0	9.0	0.126	5.5	70.2	0.158
420	3.9	2.2	0.160	3.1	15.0	0.132	4.6	60.3	0.147

and $\approx 7.8 \times 10^{19}$ cm^{-3} for the SC and DC heterostructures, respectively. The sheet carrier density can be calculated from the electron distributions. The 2DEG carrier density of SC and DC heterostructures are calculated to be 7×10^{12} and 1.7×10^{13} cm^{-2}, respectively, which is consistent with the Hall measurements sheet carrier concentration density (5.2×10^{12} and 1.8×10^{13} cm^{-2} for SC and DC heterostructures) values.

In order to find the carrier concentration depth profiles of the SC and DC heterostructures, we applied the C–V profiling technique at room temperature [23–25]. The C–V measurement allows one to measure the carrier concentration, $N_{C\text{-}V}$, as a function of depth, z, where [24],

$$N_{C\text{-}V} = \frac{C^3}{q\varepsilon_0\varepsilon}\left(\frac{dV}{dC}\right) \tag{1}$$

and

$$z_{C-V} = \frac{\varepsilon_0\varepsilon}{C} \tag{2}$$

where V is the voltage applied to the Schottky contact, C is the measured differential capacitance per unit area, and ε is the dielectric constant of the material (taken as 9.8 for $Al_{0.83}In_{0.17}N$) ($\varepsilon_0 = 8.85 \times 10^{-14}$ C/V cm; $q = 1.6 \times 10^{-19}$ C). For a non-compensated, homogeneously doped semiconductor, the carrier concentration, calculated from the C–V measurement, can be taken as equal to the free carrier concentration ($N_{C\text{-}V}(z) \cong n(z)$) [24]. The sheet carrier concentration n_s, can be calculated by integrating $N_{C\text{-}V}(z)$. This property of the C–V technique is very useful and enables the determination of the sheet carrier concentration n_s and of the location of the 2DEG in the AlInN/AlN/GaN SC and AlInN/AlN/GaN/AlN/GaN DC heterostructures. Fig. 3(a) shows the C–V characteristics measured at 1 MHz on the Schottky contact capacitors of both AlInN/AlN/GaN SC and AlInN/AlN/GaN/AlN/GaN DC heterostructures. The carrier concentration depth profiles, which were obtained from C–V measurements, of both SC and DC heterostructures are shown in the Fig. 3(b). From this figure, the maximum electron density corresponds to the location of the 2DEG channel at the single channel heterostructure in AlN/GaN interface, which is $\approx$12.7 nm below the surface. For DC sample the maximum electron density is at the AlN/GaN interface (in the second channel) and $\approx$23.5 nm below the surface. The maximum electron concentration values of the 3DEG are approximately on the order of $\approx 6.8 \times 10^{19}$ cm^{-3} and $\approx 8.0 \times 10^{19}$ cm^{-3} for the SC and DC heterostructures, respectively. With the integration of the $N_{C\text{-}V}(z)$ curve, the carrier density of SC and DC heterostructures are extracted to be 3.6×10^{12} and 8.9×10^{12} cm^{-2}, respectively, which are consistent with the calculated carrier concentration data and obtained from the Hall measurements. The value of the carrier density in the DC heterostructure is slightly larger than that in the SC heterostructure.

In general, the relationship between the applied bias-voltage and the current of the Schottky diodes, based on the TE theory, is given by [7,14],

$$I = I_{\text{thermionic}}\left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right] \tag{3}$$

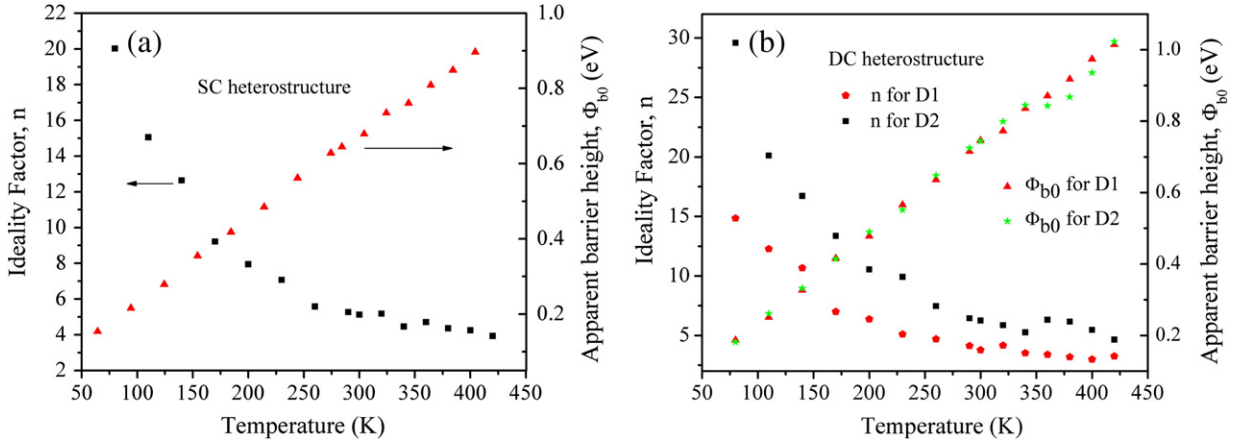

Fig. 5. Temperature dependence of the ideality factor (n) and apparent barrier height (Φ_{b0}) for Schottky contacts on (a) SC and (b) DC heterostructures, respectively.

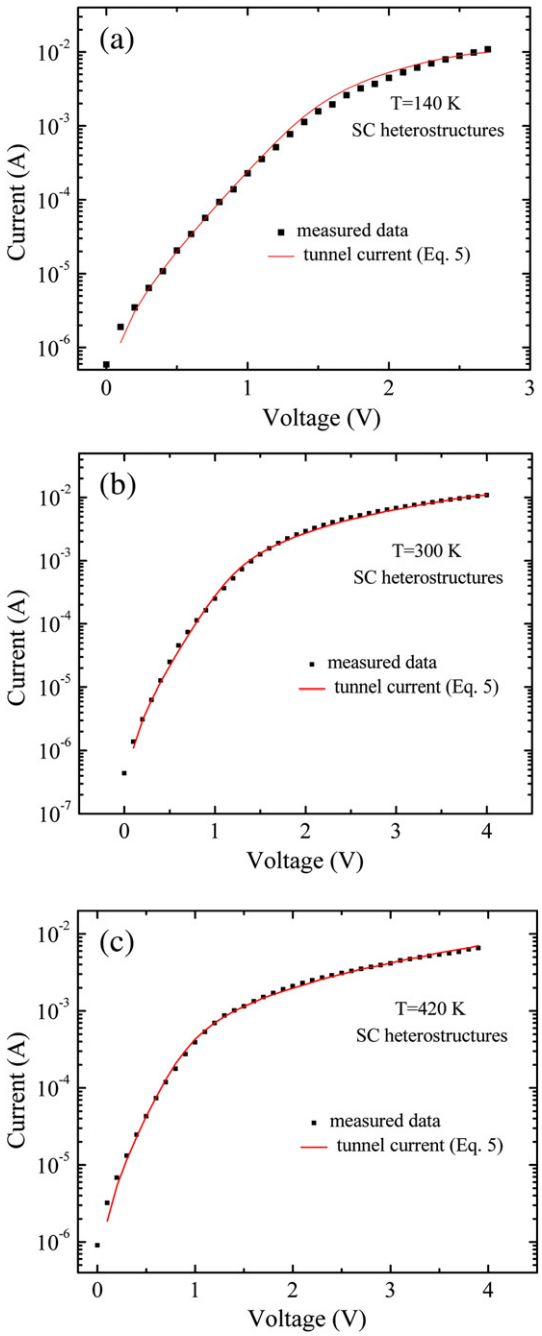

Fig. 6. The least square fits of the tunneling equation (Eq. (5)) to the semi-log *I–V* data measured at (a) 140 K, (b) 300 K and (c) 420 K for Schottky contacts on AlInN/AlN/GaN SC heterostructure.

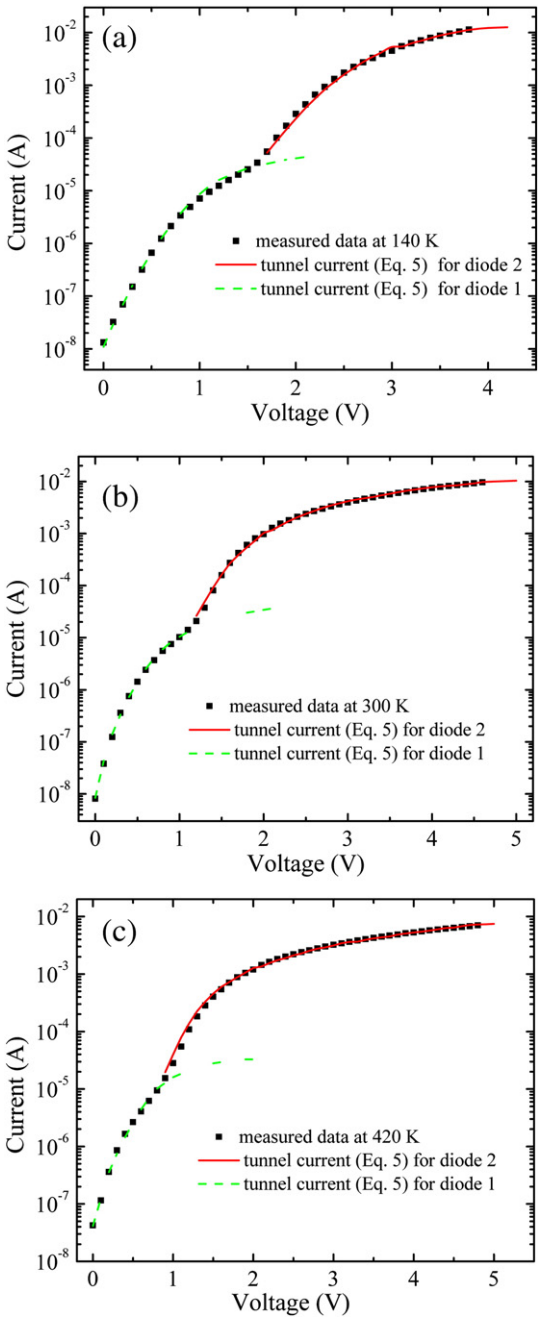

Fig. 7. The least square fits of the tunneling equation (Eq. (5)) to the semi-log *I–V* data measured at (a) 140 K, (b) 300 K and (c) 420 K for Schottky contacts on AlInN/AlN/GaN/AlN/GaN DC heterostructure.

where $I_{\text{thermionic}}$ is the reverse saturation current derived from the straight line region of the forward bias current intercept at a zero bias, and is given by

$$I_{\text{thermionic}} = AA * T^2 \exp\left(-\frac{q\Phi_{b0}}{kT}\right), \tag{4}$$

where A is the Schottky contact area, $A*$ is the effective Richardson constant (55.7 A/cm^{2}K^2 for undoped $Al_{0.17}In_{0.83}N$) [14], T is the absolute temperature in Kelvin, q is the electron charge, Φ_{b0} is the zero-bias apparent Schottky barrier height, n is the ideality factor, k is the Boltzmann's constant, V is the applied bias voltage, and IR_s is the voltage drop across resistance of the structure.

The tunneling current through the barrier is given by [7–15],

$$I = I_{tunnel}\left\{\exp\left[\frac{q(V-IR_s)}{E_0}\right]-1\right\} \tag{5}$$

where, I_{tunnel} is the tunneling saturation current and E_0 is the tunneling energy parameter.

3.1. The model

In this study, we adopted the model, which was used for GaAs Heterojunction MODFET and HIGFET characteristics by Chen et al. [20], for Schottky contacts on AlInN/AlN/GaN SC and AlInN/AlN/GaN/AlN/GaN DC heterostructures. The energy band diagram for Schottky contacts

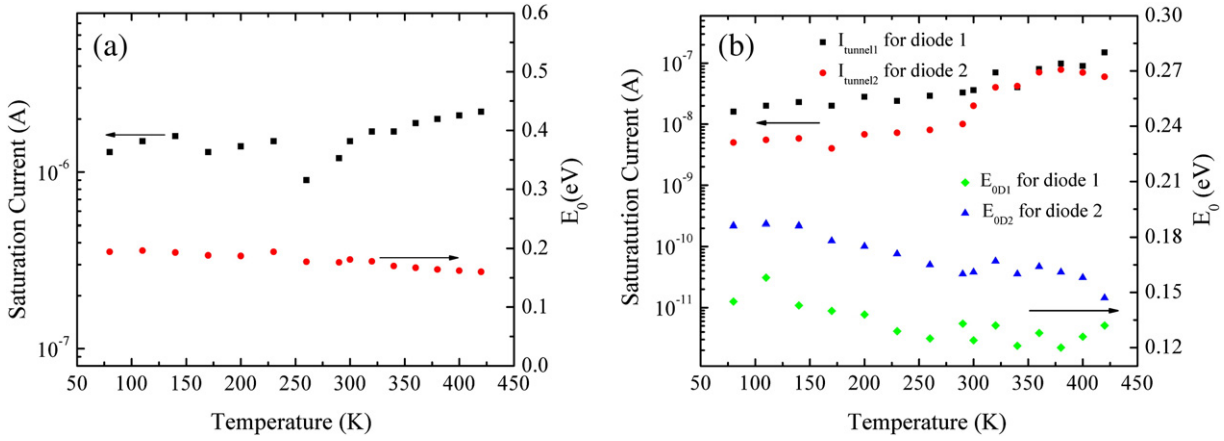

Fig. 8. Temperature dependence of tunneling saturation current I_t, and tunneling parameter E_0, which were calculated from tunneling current equation fits to the measured *I–V* data, for Schottky contacts on (a) AlInN/AlN/GaN SC and (b) AlInN/AlN/GaN/AlN/GaN DC heterostructures.

on AlInN/AlN/GaN SC and AlInN/AlN/GaN/AlN/GaN DC heterostructures at zero applied voltage (in equilibrium) is shown in Fig. 2(a) and (b), respectively. In SC heterostructure, ϕ_D is the barrier height for the metal–AlInN interface (Fig. 2(a)). In the DC heterostructure, ϕ_{D1} and ϕ_{D2} are the barrier heights for the metal–AlInN and AlN–GaN interfaces, respectively (Fig. 2(b)). In SC heterostructure, we consider an equivalent of one Schottky diode due to the heterojunction between the metal and semiconductor (AlInN) contact. On the other hand, in the DC heterostructure, we used two equivalent Schottky diodes in series: one is a metal–semiconductor (AlInN) Schottky diode and the other is the equivalent Schottky diode due to the heterojunction between the AlN and GaN. This model was used to describe the current–voltage characteristics.

From the energy band diagram given in Fig. 2(b), starting from the Schottky contact to the 2DEG, we consider two diodes back-to-back. When the positive voltage is applied to the Schottky contact and the 2DEG is grounded, the Schottky (metal–AlInN) diode (herein, it is called diode 1 and the voltage across it V_1) is forward biased and the other diode (the AlN–GaN interface, it is called diode 2 with voltage V_2) is reverse biased, and the all of the applied voltage will drop across diode 2. Because of the lower values of first barrier height (metal–AlInN) than the second diode barrier height (AlN–GaN interface) (typically, about 3.26 eV for the first one and 2.70 eV for the second one), the saturation current I_{s1} of the first diode gets smaller values than the second one. That is, when the diode 1 is forward-biased and the diode 2 is reverse biased, the resistance across the first diode becomes larger than the second one. Hence, most of the applied voltage will drop across diode 1 at low applied bias. For example at 80 K, in the low voltage range (0–1.5 V) the diode 1 is forward biased and in the medium voltage range, 1.5 up to 3.5 V, diode 2 is forward biased. The low and medium voltage ranges are changed with temperature. A detailed description of the model can be found in Ref. [20].

According to the above model description, we can model the current due to two diodes in series with the equivalent circuit elements. The current, in the DC heterostructure, through diode 1 can be written as,

$$I_1 = I_{01}[\exp(qV_1/n_1kT) - 1] \tag{7}$$

and the current through diode 2 as,

$$I_2 = I_{02}[\exp(qV_2/n_2kT) - 1] \text{ and} \tag{8}$$

$$V_T = V_1 + V_2 + I_T * R_s \tag{9}$$

where R_s is the ohmic–Schottky parasitic series resistance. V_1 and V_2 are the voltage drops across the first and second diodes, V_T and I_T are the total voltage drops and total current passed across the Schottky contact on DC heterostructure, respectively.

Fig. 4 compares a set of semi-logarithmic forward bias *I–V* characteristics of a (a) SC and (b) DC heterostructures that were measured in the temperature range of 80–420 K. In the SC *I–V* curves of the heterostructures, only one barrier height region is seen. However, the curve measured for the DC heterostructure sample, shown in Fig. 4b, indicates two distinct barrier height regions. We can distinguish two different voltage component regions: a low voltage (0–1.6 V) component region and a medium voltage region (1.6–3 V) for the measured data at 80 K. However, the low voltage region and medium voltage region changed with temperature. For example, at 420 K, the low temperature region appears between 0 and 0.9 V and the medium voltage region measured between 0.9 and 3 V ranges. The barrier heights, ideality factors, saturation current densities, and series resistances of the first and second diodes can be extracted for the two regions of the *I–V* characteristics of the DC heterostructure independently.

The values of the ideality factor (n) were obtained from the slope of the linear region of *I–V* plots for SC, and we extracted the n values in the two regions of the *I–V* characteristics of the DC heterostructure independently. The n values are seen in Table 2 and the temperature dependence behaviors are given in Fig. 5(a) and (b). The n values were found to be a strong function of temperature in both SC and DC samples. The n values for the SC heterostructure was found to increase with decreasing temperature ($n = 20.0$ at 80 K, $n = 3.9$ at 420 K). On the other hand, the ideality factor values for the first and second diodes of the DC sample were found as $n = 14.8$ at 80 K and $n = 3.1$ at 420 K, and $n = 29.6$ at 80 K and $n = 4.6$ at 420 K, respectively. The apparent SBH (Φ_{b0}) values were calculated by using Eq. (4). The Φ_{b0} versus temperature is shown in Fig. 5 for Schottky contacts on both SC and DC heterostructures. The calculation results showed that the SBHs values of the Schottky contacts SC heterostructure are $\Phi_{b0} = 0.15$ and $\Phi_{b0} = 0.89$ eV at 80 and 420 K, respectively. Similarly, the Φ_{b0} values for the first and second diodes of Schottky contacts on the DC sample were found as $\Phi_{b0} = 0.19$ eV at 80 K and $\Phi_{b0} = 1.01$ eV at 420 K, and $\Phi_{b0} = 0.18$ eV at 80 K and $\Phi_{b0} = 1.02$ eV at 420 K, respectively. As seen in Fig. 5(a) and (b), the SBHs were found to be a strong function of temperature and show the unusual behavior of increasing linearly with an increase in temperature from 80 K to 420 K for all of three Schottky contacts. Similar temperature dependent behaviors were reported in an early study for GaN based MS contacts [11,12,14–19]. The ideality factor n is a measure of conformity of the diode to thermionic emission and requires the n to be constant for different temperatures and close to 1 [7]. However, the strong increase in the barrier height with increased temperature cannot be explained theoretically. As demonstrated in an earlier study, the ideality factor n is very high (Table 2),

which indicates that the main current mechanism in the both SC and DC heterostructures is associated with carrier tunneling current rather than thermionic emission current [7–19].

The tunneling equation (Eq. (5)) was fitted to the experimental semi-log *I–V* characteristics measured for Schottky contacts on AlInN/AlN/GaN SC and DC heterostructures, by taking the I_{tunnel}, the E_0 and the R_s as adjustable fit parameters, and a fitting process was done over a wide range of applied biases (approx. 0–4 V) and at different temperatures (Figs. 6 and 7). A standard software package was utilized for the curve fitting. The measured *I–V* data, for the DC heterostructure, were separated into two different voltage regions and the tunnel current equation was fitted to each voltage region. As shown in Figs. 6 and 7, there is an excellent agreement between the measured *I–V* data and the current transport expressions for the tunneling mechanism at all temperature ranges. The E_0 and I_{tunnel} values, as determined from the fits of the tunneling current expression to the measured *I–V* data set, are summarized in Table 2.

According to the fitting process, the values of the tunneling parameter, obtained for SC heterostructure, vary from 194 meV (at 80 K) to 160 meV (at 420 K). In the DC samples, we distinguish different exponential current regimes. In DC heterostructure, the tunneling parameter, measured at a lower forward bias, changes between 120 to 145 meV. On the other hand, E_0 values, for the medium voltage region, vary between 147 and 186 meV. The typical values reported for E_0 have been in the range of 50–220 meV given for GaN-based devices such as light emitting diodes [16–19]. These characteristic energies are comparable to those that have been previously reported [16–19]. Reynolds et al. [17], reported on the electrical characteristics of the InGaN-based light emitting diodes grown heteroepitaxially. In their study, they calculated the high tunneling energy parameter (187 meV for electrons) in the low forward bias region. They also proposed this tunneling component to be related to deep levels in the vicinity of mixed/screw dislocations. Cao et al. [19] showed that these dislocations can be electrically and optically active in these alloys. In our case, it can be concluded that, at both low and medium bias for DC and SC heterostructures, data are consistent with electron tunneling to deep levels in the vicinity of mixed/screw dislocations.

Fig. 8(a) and (b) shows a plot of I_{tunnel} and E_0 versus temperature from 80 to 420 K, and in Fig. 8(b) the subscripts 1 and 2 refer to the low (for diode 1) and medium (for diode 2) bias regions, respectively. The results indicate that with increasing temperature the E_0 calculated for SC and DC heterostructures exhibits a fairly small change, while I_{tunnel} values show a weak temperature dependence in the temperature range of 80–420 K for both samples. It has been commonly accepted that a temperature insensitive tunneling parameter and weak temperature dependence in saturation current are typical features of a defect-assisted tunneling current in the GaN based heterostructures with high dislocation density [8,10,13–15].

As shown in Fig. 4, the forward-bias current is an exponential function of the applied-bias voltage in the intermediate voltage regime. It is clear that over a broad range of forward current, the behavior is exponential and, beyond that, the plots deviate from this behavior due to the effect of R_s. From Fig. 4, it can be clearly seen that the curves intersect at an almost common point, at such a point that current and voltage nearly have equal values and the derivative of the current with respect to temperature is zero. The intersecting voltage values are at nearly 1.5 V and 2.7 V for SC and DC heterostructures, respectively. The intersection behavior of the *I–V* curves of Schottky barrier diodes (SBDs) measured at different temperatures were discussed by some of the authors in their theoretical and experimental studies [26–31]. Among these study, Chand [26] argues that the intersection behaviors of the $\ln(I)$–*V* curves are an inherent property even of homogeneous SBDs of constant barrier height and are normally hidden due to saturation in current caused by series resistance. On the other hand, in inhomogeneous SBDs, due to temperature-dependent apparent barrier height, the crossing of $\ln(I)$–*V* curves is observable in the normal range. The intersection of $\ln(I)$–*V* curves may occur because of decreasing apparent barrier height with decreasing temperature, which was also supported by Osvald [27]. According to Osvald's [28] theoretical analysis, he found out the *I–V* curves of such small diodes measured at different temperatures should intersect and consecutively at higher voltages larger current flows through the diode at lower temperatures (at 100 K). He shows that the presence of the series resistance is a necessary condition of the observation of intersection behaviors in *I–V* curves. However, the intersection voltage values increase with the value of the series resistance. He argues that, if we want to observe the intersection of $\ln(I)$–*V* curves, we have to lower the diode dimensions practically to the nanometer scale. For larger dimensions, the intersection is shifted to a higher voltage region, where *I–V* curves are not commonly measured. Ravinandan et al. [31] reported that, by experimenting, they found an intersection point in the forward bias *I–V* characteristics of the Au/Pd/n–GaN SBDs. They attributed this intersection behavior to the saturation effects of series resistance in each elementary barrier. Moreover, Horvath et al. [30] reported that by experimenting they found an intersection point in the forward bias *I–V* characteristics of the Al/SiO_2/Si structure with SiC nanocrystals. This intersection of *I–V* curves seems to be an abnormality when compared to the conventional behavior of SBDs. We think that, in our Schottky contacts on AlInN/AlN/GaN SC and AlInN/AlN/GaN/AlN/GaN DC heterostructures, the deviation from linearity and intersecting behavior in the forward bias *I–V* characteristics originates from the series resistance.

4. Conclusion

In conclusion, we have studied the current-transport mechanism in the Schottky contacts on AlInN/AlN/GaN SC and AlInN/AlN/GaN/AlN/GaN DC heterostructures over a wide range of temperatures (80–420 K) and bias voltage. In DC heterostructure, two different voltage regions were observed. In order to determine the current mechanisms for SC and DC heterostructures; we fit the analytical expression given for the tunneling current to the experimental *I–V* data over a wide range of applied biases and at different temperatures. We observed a weak temperature dependence of the saturation current and a fairly small dependence on the temperature of the tunneling parameters in this temperature range. The results indicate that the mechanism of charge transport in the Schottky contacts on AlInN/AlN/GaN SC and AlInN/AlN/GaN/AlN/GaN DC heterostructures is electron tunneling to deep levels in the vicinity of mixed/screw dislocations in the temperature range of 80–420 K.

Acknowledgments

This work is supported by the projects DPT-HAMIT, ESF-EPIGRAT, EU-N4E, and NATO-SET-181, and TUBITAK under Project Nos. 107A004, 107A012, and 109E301. One of the authors (E.O.) also acknowledges partial support from the Turkish Academy of Sciences.

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